Electronic Version
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Claims

[c1] 1. A triple well electrostatic discharge (ESD) network comprising:
a substrate of a first conductivity;
an insulator region residing on the surface of the substrate;
a first region of a second conductivity being partially embedded in the insulator region and the substrate;
a second region of the second conductivity being completely embedded in the substrate and partially embedded in the first region;
a third region of the second conductivity being partially embedded in the insulator region, the substrate, and the second region;
a fourth region of the first conductivity being embedded in the insulator region and being located between the first and third regions; and
an isolation region forming a metallurgical junction between the fourth region and the first, second and third regions for the conduction of electrostatic discharge.

[c2] 2. The triple well ESD network of claim 1 wherein the isolation region abuts the top surface of the second re-

gion, an edge of both of the second and third regions and the bottom of the fourth region.

[c3] 3. The triple well ESD network of claim 2 wherein the first conductivity is p doped and the second conductivity is n doped.

[c4] 4. The triple well ESD network of claim 1 wherein the fourth region operates in the capacity of a cathode, and the first, second, and third regions operate in the capacity of an anode.

[c5] 5. The triple well ESD network of claim 1 further comprising:
a fifth region of the second conductivity located between the first and fourth regions, embedded in the insulator, and having its bottom surface abutting the isolation region; and
a sixth region of the second conductivity located between the third and fourth regions, embedded in the insulator, and having its bottom surface abutting the isolation region.

[c6] 6. The triple well ESD network of claim 1 further comprising:
a plurality of first, second, third, and fourth regions and isolation regions forming a plurality of triple well diodes

where each one of the third regions is coupled to the fourth region of a subsequent triple well diode.

[c7] 7. The triple well ESD network of claim 1 further comprising:
a fifth region of the second conductivity being completely embedded in the substrate and partially embedded in the third region;
a sixth region of the second conductivity being partially embedded in the insulator region and the fifth region;
a seventh region of the first conductivity being embedded in the insulator region; and
an additional isolation region forming a metallurgical junction between the seventh region and the third, fifth and sixths regions for the conduction of electrostatic discharge.

[c8] 8. The triple well ESD network of claim 7 wherein the additional isolation region is abutting the top surface of the fifth region, an edge of both the third and sixth regions, and the bottom of the seventh region.

[c9] 9. The triple well ESD network of claim 1 further comprising:
a sixth region of the second conductivity being partially embedded in the insulator region and the second region;
a seventh region of the first conductivity being embed-

ded in the insulator region; and
an additional isolation region forming a metallurgical junction between the seventh region and the third, second and sixths regions for the conduction of electrostatic discharge.

[c10] 10. A semiconductor device comprising:
a substrate;
an insulator residing on top of the substrate;
an n region embedded in the substrate;
a first n well embedded in the insulator and partially embedded in the n region;
a second n well embedded in the insulator and partially embedded in the n region;
a p region embedded in the insulator between the first and second n wells;
an isolation region forming a metallurgical junction between the p region and the first n well, second n well, and n region for the conduction of electrostatic discharge.

[c11] 11. The semiconductor device of claim 10 wherein the p region operates in the capacity of an anode, and the first and second n wells, and n region operates in the capacity of a cathode.

[c12] 12. The semiconductor device of claim 10 further com-

prising:

a third n well located between the first n well and the p region, embedded in the insulator, and having its bottom surface abutting the isolation region;

a fourth n well located between the p region and the second n well, embedded in the insulator, and having its bottom surface abutting the isolation region.

[c13] 13. The semiconductor device of claim 11 further comprising:

a plurality of first, second, third, and fourth n wells, embedded n region the p region, and insulator where each one of the fourth and p regions are tied one to another forming a plurality of diodes.

[c14] 14. The semiconductor device of claim 10 further comprising:

a plurality of first and second n wells, embedded n region, p region, and insulator where each one of the second n wells is tied to a succeeding first n well so as to form a plurality of diodes.